Appl. No. 10/695,363
Amdt. dated May 12, 2006
Reply to Notice of Panel Decision of April 6, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A storage system, comprising:

a storage controller for managing transfers of data between a host and storage memory;

a data mover coupled to the storage controller, the data mover handles data transferred between the host and the storage memory; and

a buffer coupled to the data mover for storing data being transferred between the host and the storage memory;

wherein, to conserve power, the storage controller ~~modifies operation~~ selectively turns off a portion of the storage system based on an amount of data in the buffer ~~status of the data transfer,~~

~~wherein the storage controller modifies operation of the storage system by turning off a portion of the storage system~~.

2. (Currently amended) The storage system of claim 1 wherein the storage controller ~~modifies operation~~ selectively turns off a portion of the storage system based on a capacity of the buffer.

3. (Canceled).

4. (Currently amended) The storage system of claim 1 wherein data is transferred between the data mover and host at a first transfer rate, and data is transferred between the data mover and storage memory at a second transfer rate, and wherein the storage controller ~~modifies operation of the storage system by functioning to~~ selectively matches the first and second transfer rates.

5. (Original) The storage system of claim 1 further comprising:

a storage memory interface coupled to the data mover, the storage memory interface handles data transferred to and from storage memory, the storage memory interface also including error correction logic.

6. (Currently amended) The system of claim 5 wherein the storage controller ~~modifies operation of the storage system by turning~~ turns off the error correction logic of the storage memory interface in the storage system if the amount of data in the buffer reaches a threshold amount.

7. (Currently amended) The system of claim 5 wherein the error correction logic of the storage memory interface comprises:

an encoder for encoding data to be stored in storage memory; and

a decoder for decoding data retrieved from storage memory;

wherein the storage controller ~~modifies operation of the storage system by turning~~ turns off the decoder in the error correction logic of the storage memory interface if the amount of data in the buffer reaches a threshold amount.

8. (Original) The system of claim 7 wherein the storage controller turns off the decoder by disconnecting power to the decoder.

9. (Original) The system of claim 7 wherein the storage controller turns off the decoder by disconnecting a clock signal to the decoder.

10.-24. (Canceled).

25. (New) A storage system, comprising:

a storage controller for managing transfers of data between a host and storage memory;

a data mover coupled to the storage controller, the data mover handles data transferred between the host and the storage memory; and

a buffer coupled to the data mover for storing data being transferred between the host and the storage memory;

wherein, to conserve power, the storage controller the selectively turns off a portion of the storage system while data is being transferred from the buffer.

26. (New) The storage system of claim 25 further comprising a storage memory interface coupled to the data mover and the storage memory, the storage memory interface having an error correction decoder.

27. (New) The storage system of claim 26 wherein the storage controller selectively turns off the error correction decoder while data is being transferred from the buffer.

28. (New) The storage system of claim 26 wherein the storage controller selectively turns off the error correction decoder based on a fill status of the buffer.

29. (New) The storage system of claim 26 wherein the storage controller selectively turns on the error correction decoder based on a fill status of the buffer.

30. (New) The storage system of claim 25 wherein data is transferred between the data mover and host at a first transfer rate, and data is transferred between the data mover and storage memory at a second transfer rate, and wherein the storage controller selectively matches the first and second transfer rates to pipeline data.

31. (New) The storage system of claim 30 wherein the storage controller dynamically selects between turning off a portion of the storage system while data is transferred from the buffer and matching the first and second transfer rates to pipeline data.

32. (New) The system of claim 27 wherein the storage controller turns off the error correction decoder by disconnecting power to the error correction decoder.

33. (New) The system of claim 27 wherein the storage controller turns off the error correction decoder by disconnecting a clock signal to the error correction decoder.

34. (New) The system of claim 25 wherein the storage controller turns on a portion of the storage system when a subsequent transfer of data is initiated by the storage system.

35. (New) The system of claim 25 wherein the storage controller adjusts the rate of transfer of data between the host and the storage memory based on a remaining capacity of the buffer.

36. (New) The system of claim 35 wherein the storage controller determines when the remaining capacity of the buffer is increasing and decreasing.

37. (New) The system of claim 35 wherein,

if the remaining capacity of the buffer is decreasing, the storage controller decreases the transfer rate between the host and the storage memory; and

if the remaining capacity of the buffer is increasing, the storage controller increases the transfer rate between the host and the storage memory.